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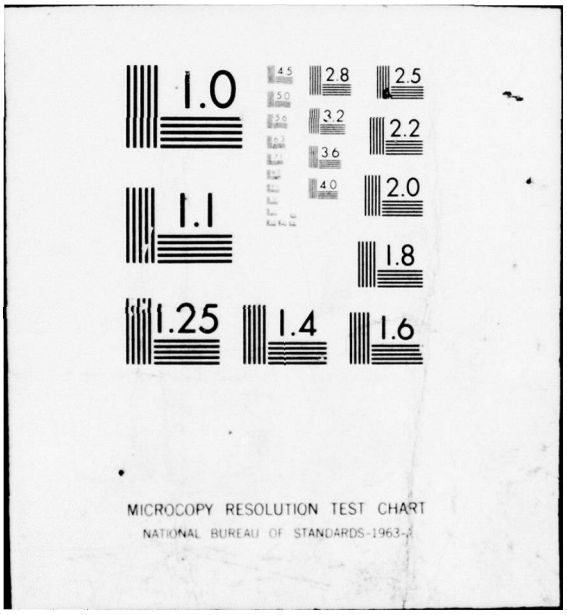
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Report No. 03-69-35

GaAsP INFRARED LIGHT SOURCES

Final Report

by

George A. Henderson and David W. Treat

October 1969

U.S. Army Electronics Command
Night Vision Laboratory
Fort Belvoir, Virginia 22060

TEXAS INSTRUMENTS INCORPORATED
P. O. Box 5012
Dallas, Texas 75222

Contract No. DAAK02-69-C-0084

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SUMMARY

Investigations were performed in an effort to extend the state-of-the-art of GaAsP light emitters and emitter arrays. This effort included a materials study aimed at providing usable GaAsP capable of yielding high quantum and power efficiency at the desired wavelength. The effort also consisted of a study of processing and fabrication techniques to take full advantage of the material capabilities. At the present time, the problem of device degradation has been found to be the main area in which further effort is required.

FOREWORD

For the past several years, a program of device fabrication and evaluation has been conducted at Texas Instruments for the Night Vision Laboratory, Fort Belvoir, Virginia. The program has been devoted to semiconductor light emitting devices fabricated from GaAsP material. The first portion of this work was carried out under U. S. Army Contract No. DAAK02-67-C-0583. The work done under this contract was reported in Interim Report No. 03-68-20 and in Final Report No. 03-68-56.

The second phase of work performed at Texas Instruments on GaAsP emitting diodes was done under U. S. Army Contract No. DAAK02-69-C-0084. The purpose of this document is to report the results of the work done on this second contract.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I

MATERIALS DEVELOPMENT

A. BASIC GOALS

The objective of the materials development effort expended during the course of this contract has been to investigate certain variable parameters of the $GaAs_{1-x}P_x$ crystal growth process. While the process used in this laboratory to produce device-quality slices of $GaAs_{1-x}P_x$ was sufficiently advanced and considered beyond the experimental (or feasibility study) stage, much developmental work remained to be done to enlarge the scope of technological knowledge of the $GaAs_{1-x}P_x$ system. The desired goals of the present effort also included optimization of these variable crystal growth parameters by correlating these studies with the results of device performance studies carried out on hemispherically shaped light-emitting diodes fabricated from samples of the grown crystals.

B. CRYSTAL GROWTH PROCESS

The basic process used to prepare the $GaAs_{1-x}P_x$ material in slice form is an open-tube chemical vapor epitaxial deposition technique which utilizes HCl-transported gallium and mixtures of arsine (AsH_3) and phosphine (PH_3) in hydrogen as sources of reactive components.

More detailed description of systems of this type are included in reports of previous work.[1,2,3,4]

For the work described here, transparent fused-quartz reactor systems of two types were used. The horizontal, single-slice reactor (Figure 1) produced the majority of the material supplied for device evaluation and will be dealt with more extensively in the following discussion. The elbow-shaped, three-slice reactor (Figure 2) also produced device-quality material, but was principally used for doping studies and for investigations related to the higher phosphorous-content alloys of $GaAs_{1-x}P_x$.

Substrate material for this epitaxial process was obtained by sawing ⟨100⟩ oriented slices of GaAs from Czochralski-pulled single crystals. Work in the early stages of development with other substrate orientations (principally ⟨111⟩ "A" and "B") resulted in the selection of the ⟨100⟩ orientation for further process development. Both tin-doped ($n \sim 5 \times 10^{17}$) and undoped ($n \sim 10^{16}$) N-type crystals have been utilized and substrates have been obtained from crystals pulled in either the ⟨111⟩ or ⟨100⟩ direction. It was assumed that these crystals were of reasonably high dislocation density ($\sim 10^4$ to $10^5 cm^{-2}$), so no effort has been expended to categorize substrate material by means of etch pit counts.

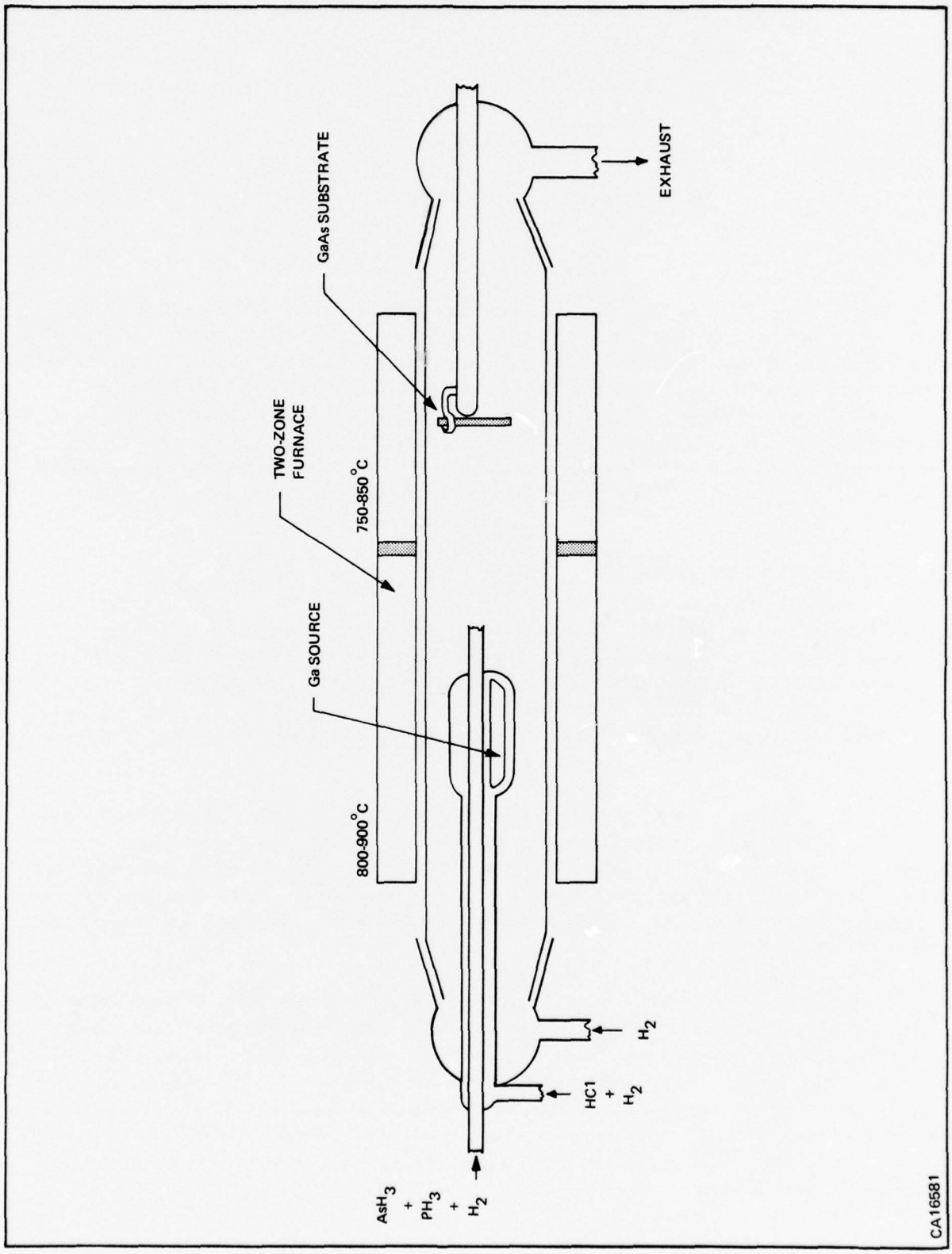

Figure 1. Horizontal Vapor-Growth System

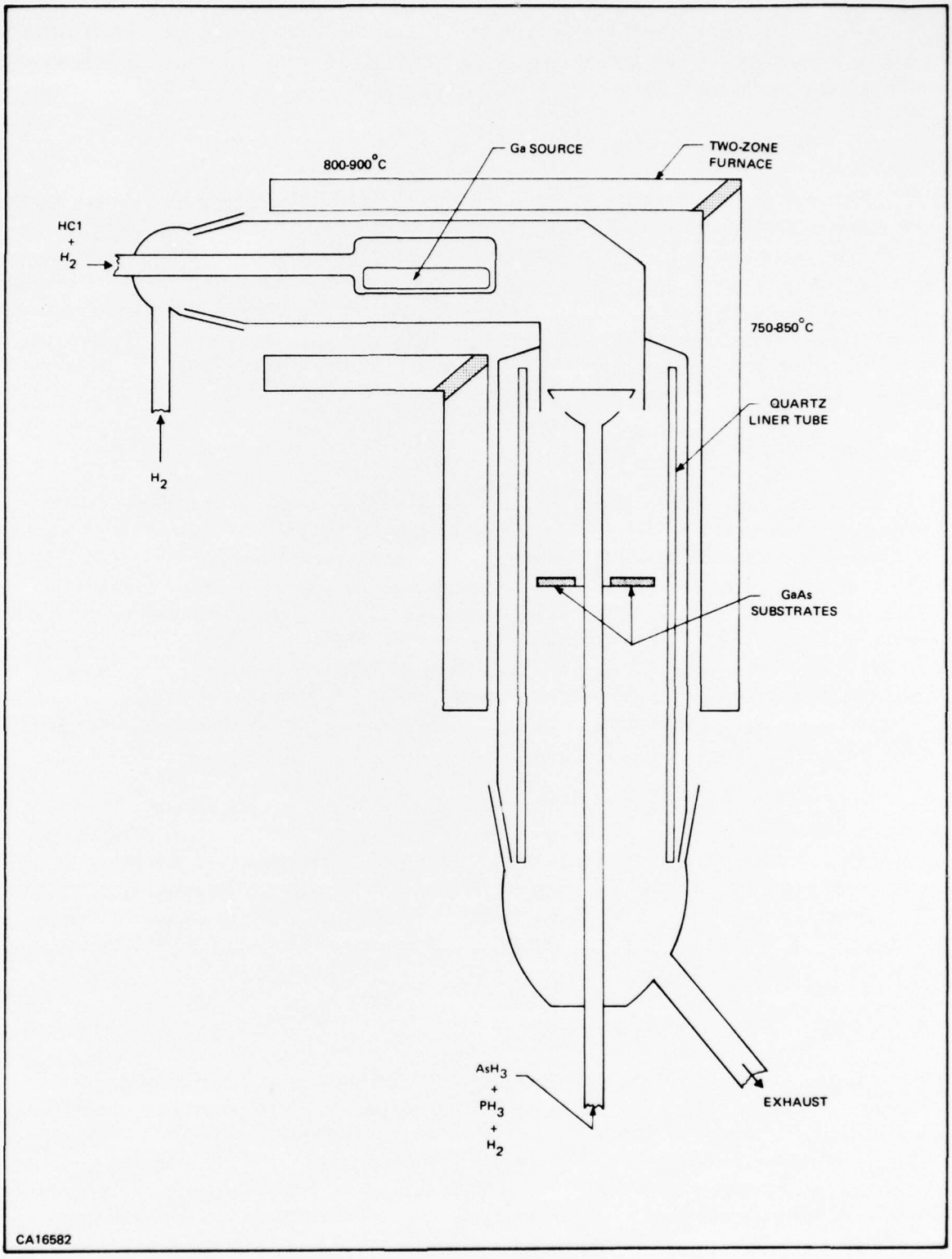

Figure 2. Elbow-Shaped Vapor-Growth System

After sawing, the substrate slices were lapped to remove sawing damage and then chemically polished using NaOCl. [5] Immediately prior to use in epitaxial growth, the substrates were given a final beaker etch using a solution of concentrated H_2SO_4, 30% H_2O_2, and H_2O (8:1:1).

1. Standard Crystal Growth Parameters

The work performed during the previous contract periods served to define certain reactor conditions as being optimum from the point of view of surface quality and reproducibility. These conditions consist of four gas flow parameters and the controlled temperature settings of the two zones of the resistance heated furnaces used. Typical conditions (hereafter referred to as standard conditions) for the horizontal reactor system were a total gas flow of about 600 cc/minute, a total reactant species concentration of ~ 2%, a Ga/Gp V ratio of ~ 2, and a vapor phase composition of ~ 6.5 to 10.0 mole % GaP. For these flow conditions, standard temperature settings of about 900°C and 825°C were used for the source and substrate zones, respectively.

2. Variations from Standard Parameters

Because the four gas flow parameters stated above are interrelated, the changing of flow rate of one reactant species affects a change in at least one other of the four. The approach was to deviate as little as possible from standard flow settings in order to maintain some predictability that the crystal growth run would result in usable crystalline material. Therefore, some unintentional, but slight variations did occur in total gas flow and total reactant species concentration during the course of these studies. These variations, ±50 cc/min in total gas flow and a range of 1.65% to 3.10% in reactant concentration, were thought to be relatively unimportant on the basis of observations made during the optimization studies carried out previously when similar variations occurred as the result of changing to cylinders of different reactant dilution, (e.g., from 2.0% to 4.0% AsH_3 mixtures in hydrogen.)

Slight variations in substrate temperature settings were occasionally necessary to provide a minimal occurrence of gross defects. Two types of defects were generally observed, either hillock formations or voids (pits) in the grown surface. As reported previously,[2] the occurrence of these gross defects (for a given set of flow conditions) appears to be related to the substrate temperature setting, with the hillocks occurring at lower temperatures than the pits. The temperature variations necessary to minimize these defects, generally within the range of ± 5°C, were considered to result in standard temperature settings.

a. Variation of Vapor Phase Composition

Previous studies of variation of this parameter were principally directed toward producing material capable of emitting light in the desired wavelength range. For gross variations in composition (> 10 mole %), it was observed that achieving optimum surface condition required an increase of substrate temperature with increasing phosphorous content. For example, epitaxial layers containing approximately 40 mole % GaP required substrate temperature settings in the vicinity of 850°C when other standard conditions were employed. Since a better understanding of the effect of graded composition alloy layers was desired (see Figure 3), a portion of this effort was

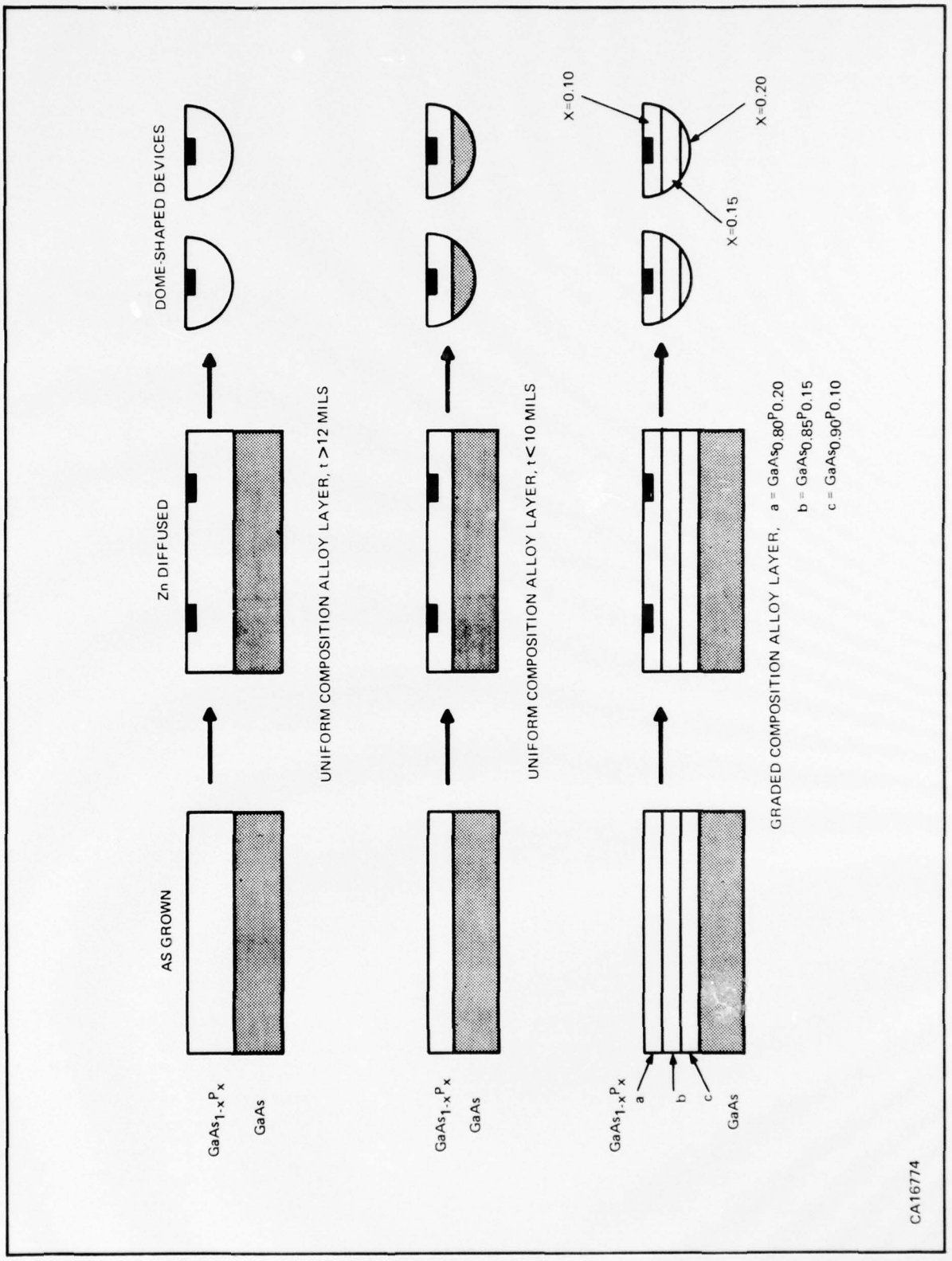

Figure 3. Typical Material Structural Configurations

directed to determining the range of compositions that could be grown satisfactorily at a single substrate temperature setting. Using standard temperature settings, alloy layers were grown from vapor compositions ranging from 6.0 to 14.0 mole % PH^3. X-ray lattice constant measurements made on these samples yielded a compositional range of 7.5 to 17.5 mole % GaP in the solid phase. As mentioned previously[2] this relationship of vapor and solid phase compositions has been observed in this laboratory, and is also reported by other investigators.[6] The relationships observed here are largely qualitative and are determined empirically for a given set of reactants, since no effort was expended to accurately determine the authenticity of the suppliers' stated gas cylinder analyses. The emission wavelength data from diodes fabricated from this material is shown with previous data in Figure 4. These studies resulted in successful application to the graded layer growth technique and several samples were supplied for device evaluation with "transparent" layers having higher phosphorous contents (by 2 to 4 mole %) than the region in which the P-N junction was formed.

b. Variation of Ga/Gp V Ratio

Since all early crystal growth work in this laboratory was performed from relatively Ga-rich vapor while other investigators apparently preferred either stoichiometric or As-rich systems[3,4], the study of the effect of variations in the Ga/Gp V ratios employed was undertaken. An additional input[7] concerning melt-grown GaAs crystals also suggested that luminescent efficiencies might be related to the arsenic pressure (or excess) in crystal growth systems. The possibility of achieving higher growth rates by varying this parameter was also considered.

During this study, Ga/Gp V (more correctly, the ratio of flow rates of pure HCl to the sum of those of AsH_3 and PH_3) ratios of 0.56, 1.0, 1.99 (std.), 3.42, 4.18, and 5.70 were employed. As mentioned above, some unintentional variation also occurred in the total reactant species concentration, ranging from 1.65 to 3.17% during these studies. In order to achieve usable surface quality on crystals grown using the varied Ga/Gp V ratios, a variation of the substrate zone temperature was found to be required. These temperatures ranged from 780°C to 850°C with increasing Ga/Gp V ratios. The tendency toward gross surface imperfections, even with the varied substrate temperatures, was much more pronounced for Ga/Gp V ratios of 1.0 or less and 4.18 or greater, which seems to confirm that the standard Ga/Gp V ratio is optimum from a surface quality viewpoint. Run-to-run variations of growth rates under standard conditions are still so poorly understood that no conclusive evidence relating growth rates to variations of the Ga/Gp V ratio could be obtained.

C. DOPING STUDIES

Intentional doping of the growing epitaxial $GaAs_{1-x}P_x$ alloy layers has been achieved in two distinctly different methods. The first method employed was used more extensively in the preparation of material evaluated during this study and consisted of adding a measured amount of elemental tin to the gallium source boat. This impurity, generally on the order of ~ 0.5 to 1.0% by weight, was then transported by the HCl along with the gallium to the deposition zone of the reactor. Control of the dopant concentration with this technique did not appear to be of the sensitivity desired, based on evaluation of the grown layer by the Point Contact Reverse Breakdown measurement technique.[8] Although some effort to vary the layer concentration by varying the Sn

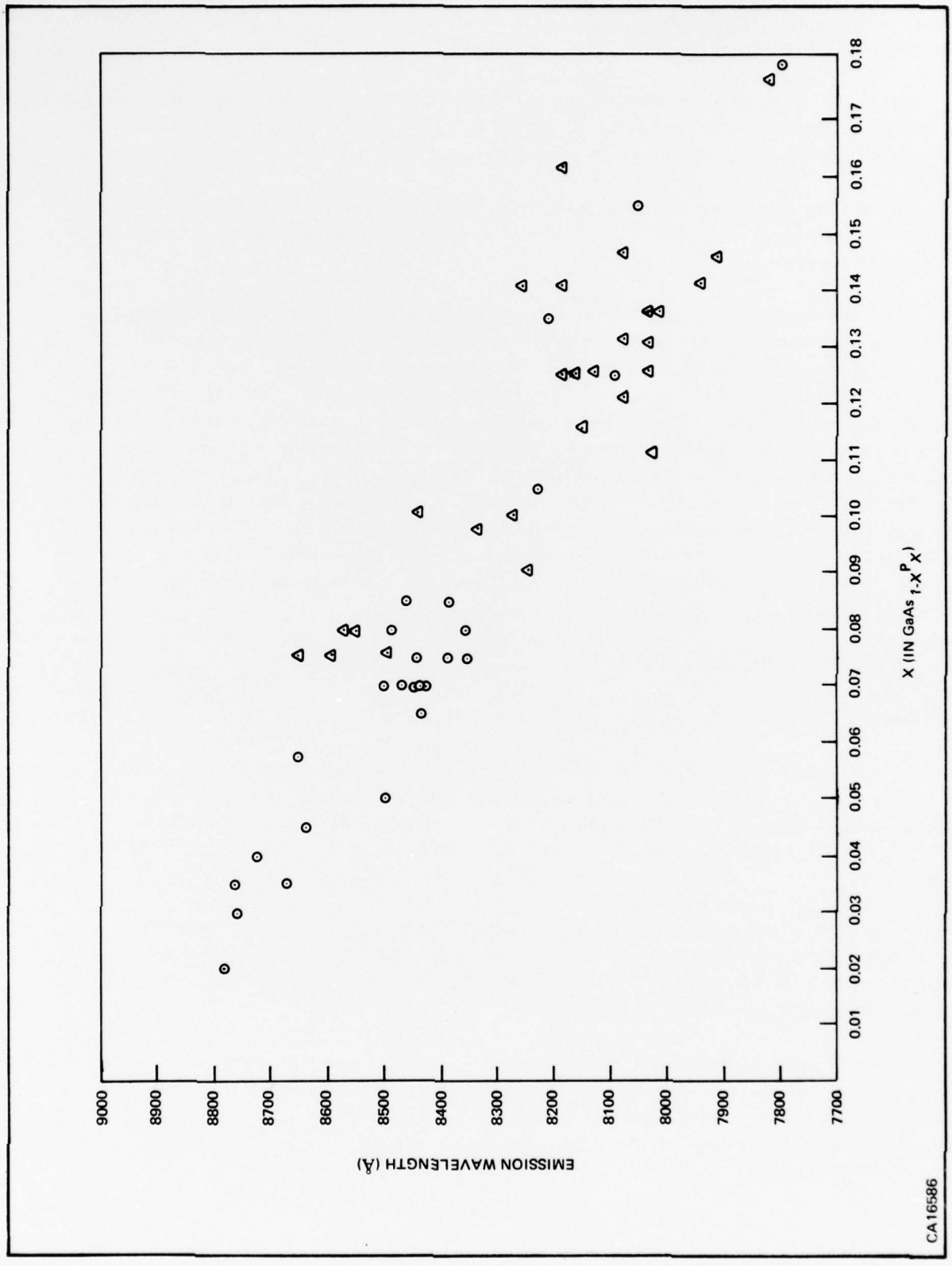

Figure 4. Emission Wavelength versus $GaAs_{1-x}P_x$ Composition

concentration in the feed source was attempted, the most predictable PCRB values (~ 5 to 8 V) were obtained by using feed sources containing 1% (wt) Sn.

The second method of doping consisted of the use of a volatile doping source. The dope gas mixture was introduced into the reactor gas stream by means of a "controlled leak" down stream from the gallium feed source to prevent its contamination.

During these studies, no effort was made to determine the actual concentration of dopant in the reactant gas stream, as the major objective was to achieve the desired impurity concentration in the epitaxial layer.

Three different dopants were investigated with this technique, sulfur as H_2S, selenium as a mixture of 1000 ppm H_2Se/hydrogen, and silicon as SiH_4. Device quality crystals doped with either sulfur or selenium were grown over a carrier concentration range from ~ 5 X 10^{16} to ~ 1 X $10^{18} cm^{-3}$. Although further work remains to be done in developing this technique, the degree of control and reproducibility of doping concentrations achieved by this method are vastly superior to those observed with the elemental tin system. Some effort was expended to grow Si-doped material with a silane doping source in the elbow-shaped reactor system. The bulk of work with this system was directed toward the growth of "pure" GaAs, but the effort was abandoned because of the inability to achieve donor concentrations greater than about 1 X $10^{16} cm^{-3}$. The very low carrier mobilities (~ 1000 cm^2-V^{-1} -sec^{-1} at room temperature) for this concentration indicated severe crystal imperfections, and further additions of silane to the reactor actually caused the epitaxial growth to become polycrystalline.

D. EVALUATION TECHNIQUES

1. Electrical Measurements

Probably the most significant achievement during the course of this work was acquiring the apparatus necessary to make Hall effect measurements on the material grown with this process. Six-armed Hall Bars were prepared from the epitaxially grown $GaAs_{1-x}P_x$ by ultrasonic cutting and indium contacts were applied and alloyed at ~ 450°C on a heater strip under a forming gas atmosphere.

A summary of the electrical properties for variously-doped samples of ~ 10 mole % GaP alloy composition is given in Table 1. These measurements were performed on epitaxial layers grown on semi-insulating GaAs substrates except in the case of the tin-doped layers, from which the substrate material was completely removed by lapping.

Although some further work could be done to increase the purity (decrease the donor concentration) of the undoped material obtainable from this system, the present materials objectives do not include extremely high purity and it is thought that the electrical properties of these undoped layers indicate a sufficiently high purity level to form an adequate basis for the preparation of material satisfactory for LED fabrication.

Table I. Electrical Evaluation of Various Slices

Sample No.	Dopant	ρ (ohm-cm)	μ ($cm^2-V^{-1}-sec^{-1}$)	nd (cm^{-3})
N10485–42	None	0.31	–5640	-3.6×10^{15}
N10485–42	(77°K)	0.085	–28,200	-2.6×10^{15}
N10485–44	None	0.22	–6105	-4.8×10^{15}
N10485–44	(77°K)	0.066	–27,600	-3.5×10^{15}
N10485–45	None	0.90	–6330	-1.1×10^{15}
N8888–106	Sn	0.041	–4500	-3.4×10^{16}
N9765–4	Sn	0.008	–2950	-2.8×10^{17}
N9765–5	Sn	0.023	–4050	-6.8×10^{16}
N9765–8	Sn	0.012	–3700	-1.4×10^{17}
N10485–11	S	0.10	–4550	-1.4×10^{16}
N10485–15	S	0.011	–3440	-1.6×10^{17}
N10485–14	S	0.003	–2120	-1.0×10^{18}
N10485–13	S	0.002	–1610	-2.2×10^{18}
N10485–51	Se	0.009	–3460	-2.1×10^{17}
N10485–56	Se	0.007	–3050	-3.1×10^{17}
N10485–52	Se	0.004	–2710	-6.0×10^{17}
N10485–53	Se	0.001	–1510	-3.8×10^{18}

The actual range of doping concentration for the tin-doped material used in device fabrication is not known. The variation in donor concentration seen in Table I is believed to be indicative of the lack of control attainable with this technique. The variation in the tin content of the feed source for these four runs was less than a factor of two, yet an order of magnitude difference in concentration was observed. The PCRB evaluation technique was also of insufficient sensitivity as the lower three samples, differing by a factor of four in donor concentrations, had indistinguishable breakdown voltages on the order of five volts. Since the lowest PCRB values observed on any of the tin-doped slices were on the order of ~ 4 to 5 V, it was concluded that the upper limit on donor concentration achievable by this technique is probably no greater than about $5 \times 10^{17} cm^{-3}$.

Variation of concentration using gaseous dopant sources was achieved by determining the "controlled leak" settings required to produce material of the desired impurity concentration range, and then estimating the donor concentration of the material supplied for device fabrication by comparison with calibration curves based on the results listed in Table I.

2. Other Evaluations

Selection of slices to be submitted for device fabrication was based on several different evaluations. To attempt to evaluate the effect of the intentional growth parameter variations which were made during this effort, some slices were processed which otherwise would have been withheld. The single, most important criteria for all material selection was the layer thickness (> 0.010 inch) measurement which was made by cleave and stain techniques. Next in importance was

some indication of satisfactory doping concentration, as deduced by either PCRB or Hall effect measurements. A visual inspection of surface quality (occurrence of gross defects) served to eliminate some slices, although several slices were processed which had either the pit or hillock type of defect when the density of these defects was minimal. Composition data provided by X-ray lattice constant determination was used on a fairly routine basis, with particular attention given to slices prepared after replacement of a cylinder of reactant gas.

In an attempt to find an analytical tool which would be capable of categorizing material independent of device fabrication processes, two nondestructive techniques were investigated. Electron microprobe cathodoluminescence studies, which have been correlated with GaAs device performance[9], were initiated on some samples of $GaAs_{1-x}P_x$, but no meaningful correlation with device performance could be deduced from the limited amount of work. X-ray Laue topography, a technique described in the literature for evaluating (Hg,Cd)Te single crystals[10], was used more extensively during the course of these studies. Widely varying patterns were seen in the topographs, ranging from a regular, geometric pattern of "crosshatching" through a distorted pattern to samples which exhibited almost no structural definition. Typical topographs are given in Figure 5. Although devices were fabricated from a number of slices on which topographs were made, there was no consistent correlation between the appearance of the topographs and device performance.

E. EVALUATION OF CRYSTAL GROWTH PROCESS VARIATIONS

The relevant crystal growth parameter variations which were undertaken during the course of this work are listed in Table II for the various slices which were submitted for device fabrication. Also given in this tabulation is the device process number which corresponds to device evaluation data given in the following section. Attempts to correlate these materials variations with device performance have thus far been futile, which seems to indicate that further efforts will need to be expended before an understanding of the key factors relating to device performance will be attained.

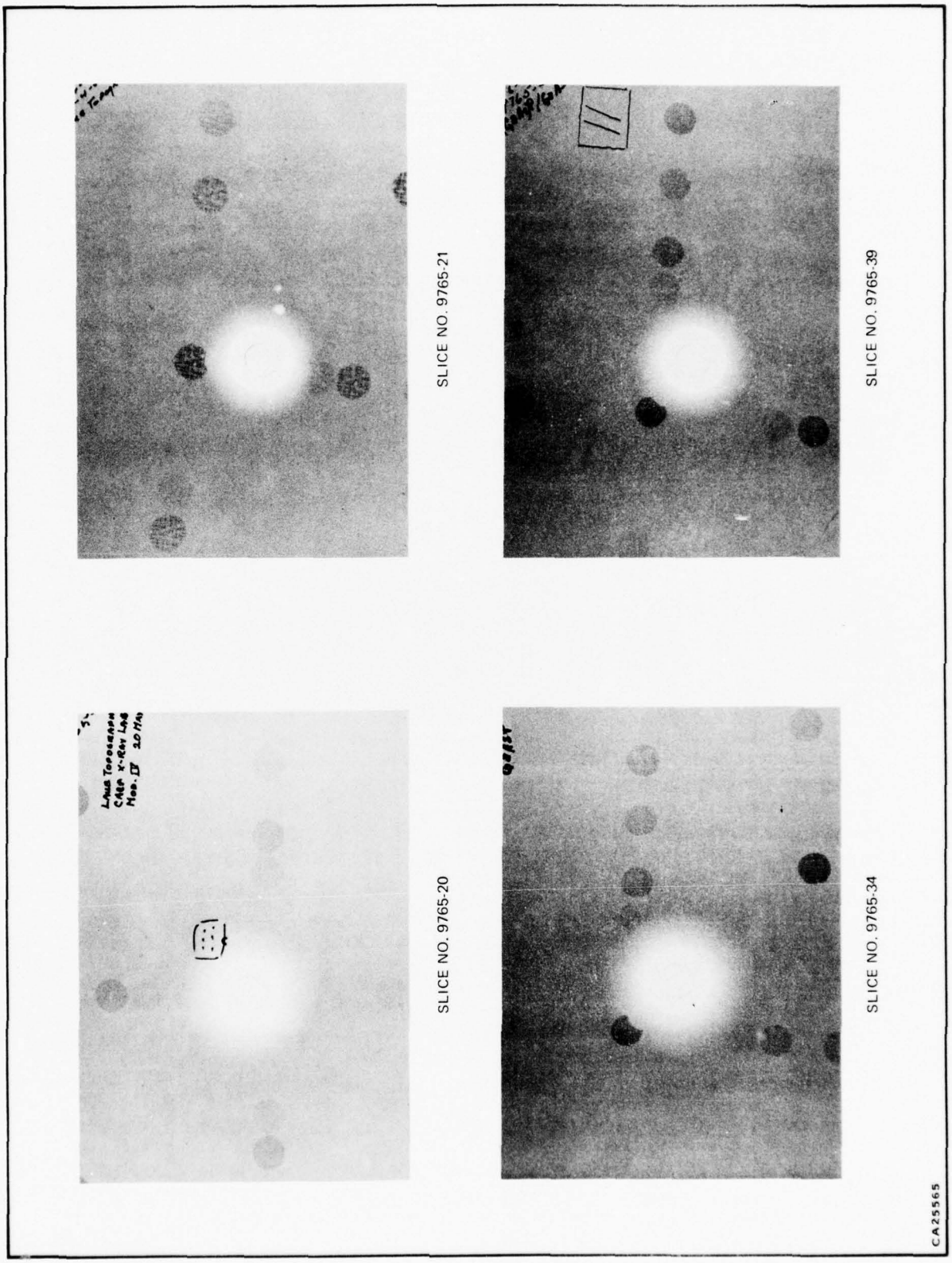

Figure 5. Selected Laue Topographs

Table II. Crystal Growth Parameters of Various Slices

Slice No.	Process No.	Compositional Structure	Dopant Concentration	Ga/Gp V
N888–107–1	1464	Uniform	Sn	1.94
N888–108–2	1465	Uniform	Sn	1.94
N888–109–3	1466	Graded	Sn	1.94
N888–110–1	1467	Graded	Sn	1.94
N888–111–1	1468	Graded	Sn	1.94
N888–108–1	6925	Uniform	Sn	1.94
N888–110–3	6924	Graded	Sn	1.94
N888–111–2	6923	Graded	Sn	1.94
N9765–11	1459	Uniform	Sn	1.44
N9765–12	1460	Uniform	Sn	1.44
N9765–13	1461	Uniform	Sn	1.44
N9765–14	1462	Uniform	Sn	1.44
N9765–15	1463	Uniform	Sn	1.44
N9765–17	1485	Uniform	Sn	2.04
N9765–19	1486	Uniform	Sn	2.04
N9765–20	1487	Uniform	Sn	2.04
N9765–21	1488	Uniform	Sn	2.04
N9765–22	1489	Graded	Sn	2.04
N9765–24	1490	Graded	Sn	2.04
N9765–29	1524	Graded	Sn	1.96
N9765–30	1518	Graded	Sn	1.99
N9765–34	1525	Graded	Sn	1.99
N9765–35	6922	Graded	Sn	1.99
N9765–37	1526	Graded	Sn	1.99
N9765–39	1527	Graded	Sn	1.99
N9765–41	6927	Graded	Sn	1.99
N9765–44	1530	Graded	Sn	1.99
N9765–48	1531	Graded	Sn	1.99
N9765–49	1532	Graded	Sn	1.99
N9765–51	1533	Graded	Sn	1.99
N9765–53	1537	Graded	Sn	1.99
N9765–66	6934	Uniform	Sn	3.42
N9765–68	1539	Uniform	Sn	3.42
N9765–69	1538	Uniform	Sn	4.18
N9765–70	1562	Uniform	Sn	4.18
N9765–75	Not Completely Processed	Uniform	Unintentionally undoped	4.18
N9765–78	Not Completely Processed	Uniform	Unintentionally undoped	5.70
N9765–80	Not Completely Processed	Uniform	Unintentionally undoped	1.99
N9765–81	Not Completely Processed	Uniform	Unintentionally undoped	1.99
N9765–85	Not Completely Processed	Uniform	Unintentionally undoped	1.99
N9765–93	1567	Uniform	Sn	1.99
N9765–102	1568	Uniform	Sn	1.00

Table II. Crystal Growth Parameters of Various Slices (Continued)

Slice No.	Process No.	Compositional Structure	Dopant Concentration	Ga/Gp V
N9765–103	1569	Uniform	Sn	1.00
N9765–107	1570	Uniform	Sn	0.56
N9765–109	1571	Uniform	Sn	0.56
N9765–111	6926	Uniform	Sn	1.99
N10485–22	6936	Uniform	S, 1×10^{17}	2.09
N10485–23	6932	Uniform	S, 1×10^{17}	2.09
N10485–24	6937	Uniform	S, 1×10^{17}	2.09
N10485–25	6938	Uniform	S, $1–5 \times 10^{16}$	2.09
N10485–26	6939	Uniform	S, $1–5 \times 10^{16}$	2.09
N10485–27	6940	Uniform	S, $1–5 \times 10^{16}$	2.09
N10485–28	6941	Uniform	S, 7×10^{17}	2.09
N10485–30	6942	Uniform	S, 7×10^{17}	2.09
N10485–32	6933	Uniform	S, 1×10^{18}	2.09
N10485–33	6935	Uniform	S, 3×10^{17}	2.09
N10485–34	6943	Uniform	S, 1×10^{17}	2.09
N10485–55	6944	Uniform	Se, 6×10^{17}	2.09
N10485–62	6945	Uniform	Se, 2×10^{17}	2.09
N10485–65	6948	Uniform	Se, 3.5×10^{17}	2.09
N10485–66	6946	Uniform	Se, 9×10^{17}	2.09
N10485–68	6947	Uniform	Se, 2×10^{18}	2.09
N10485–69	6949	Uniform	Se, 3.5×10^{18}	2.09

SECTION II

DEVICE STUDIES

A. DEVICE FABRICATION

The overall aim of the work reported here is the fabrication and characterization of hemispherical GaAsP light emitting devices. To this end, the materials effort of the previous section was coupled with an extensive program involving slice processing, device assembly, and analysis of the finished diodes. This program served both as a vehicle for producing the light emitters as well as a means of providing direct feedback of information to the materials growth area as to slice quality based on device characteristics.

The light emitters fabricated during the course of this contract were made from epitaxially deposited GaAsP N-type material. A planar zinc diffusion process was used to form the PN junctions. The diffusion is made at 925°C in a sealed quartz ampoule having a volume of 28 cm^3. The source is 2.5 mg of elemental zinc, and the junction depth is typically 4 to 6 μm. The devices have hemispherical dome geometry with a diameter of 16 to 18 mils. This structure is shown schematically in Figure 6. The PN junction is located at the center of the flat face of the hemisphere in order to eliminate total internal reflection and thereby maximize efficiency and power output.

Light is produced at the PN junction when a forward bias is applied to the device. The photons are produced by the radiative recombination of electrons injected into the P-type region. Recombination of holes injected into the N-type region is typically nonradiative.

In order to provide minimum thermal resistance consistent with matched expansion coefficients and minimum mechanical strain, silicon submounts of two different types were used in mounting the diodes to the headers. These two types of submounts are shown in Figures 7 and 8. In the first case, the P-type connection is made to the header through the low-resistivity silicon. In the second case, the bulk silicon is insulating and therefore does not form an active part of the electrical connection. All connections are made by the metallization on top of the silicon. Assembly of the dome to submount is done using 60% tin – 40% lead solder.

The discrete light emitting diodes comprising that portion of the technical delivery made under this contract were mounted on two types of headers. The ten diodes making up the first delivery were mounted on TIL09 headers. This header is shown in cross section in Figure 9. The kovar reflector is an ellipsoid of revolution and provides a beam spread of about 20° (total angle) at the half power points. The data taken at 200 mA forward bias on these ten devices is given in Table III.

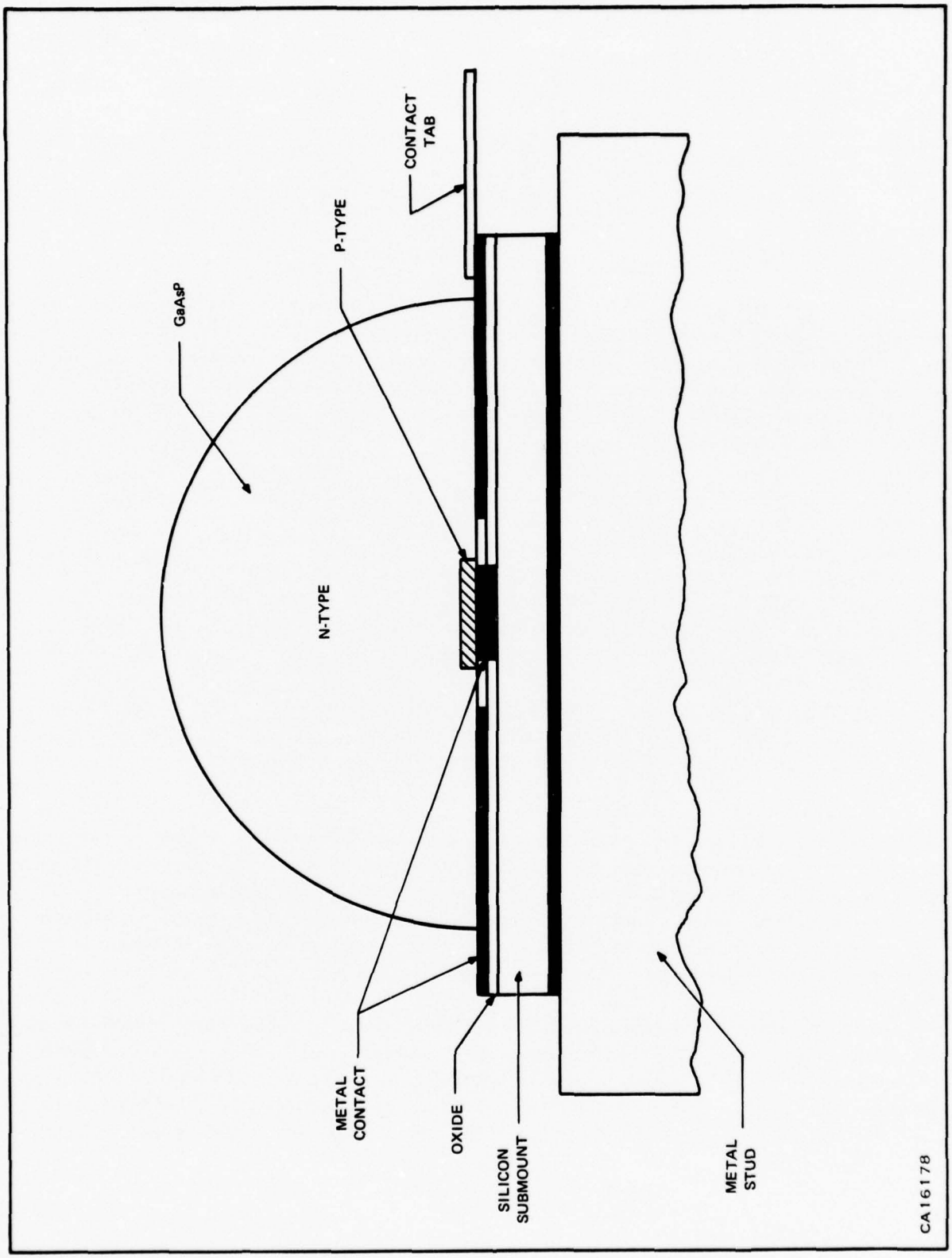

Figure 6. Geometry of Hemispherical Light Emitting Diode

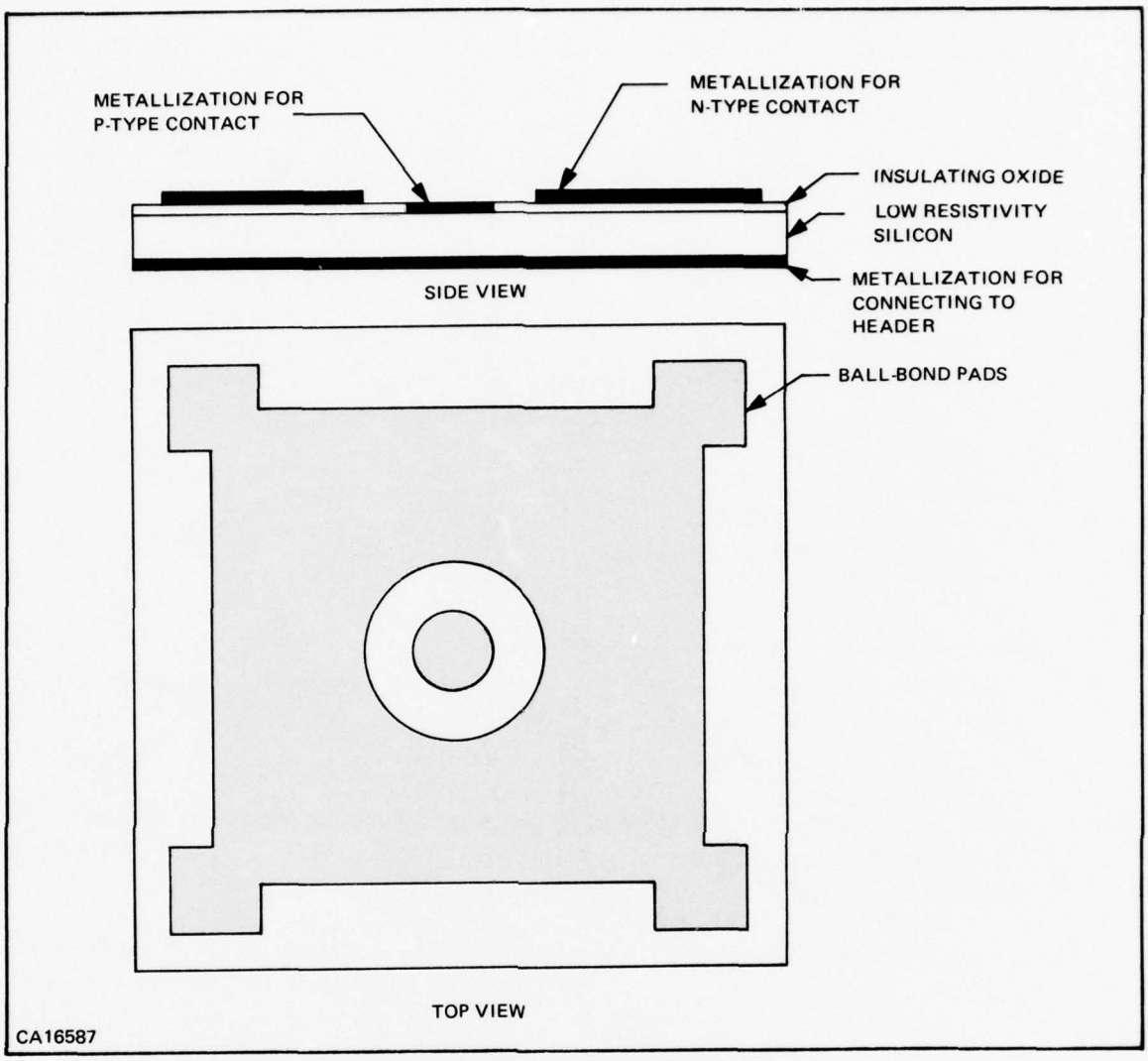

Figure 7. Schematic View of Silicon Submount

The ten discrete devices comprising the second portion of the delivery were mounted on 8-32 stud headers, shown in Figure 10. The overall length is 0.800 inch and the diameter of the top flange is 0.120 inch. The threaded end provides both the positive electrical connection and thermal path. The top flange, which is insulated by a ceramic spacer, is the negative connection. In the end view, the four gold wires which connect the submount to the top of the flange can be seen. The thickness of the flange gives no shadowing to the emitted light. The data taken on this group of devices is given in Table IV.

In addition to the 20 discrete devices delivered, two arrays of hemispherical emitters were also fabricated for delivery on the contract. Each array was composed of four diodes mounted on insulating type submounts and connected in series on a single header. This is shown in Figure 11.

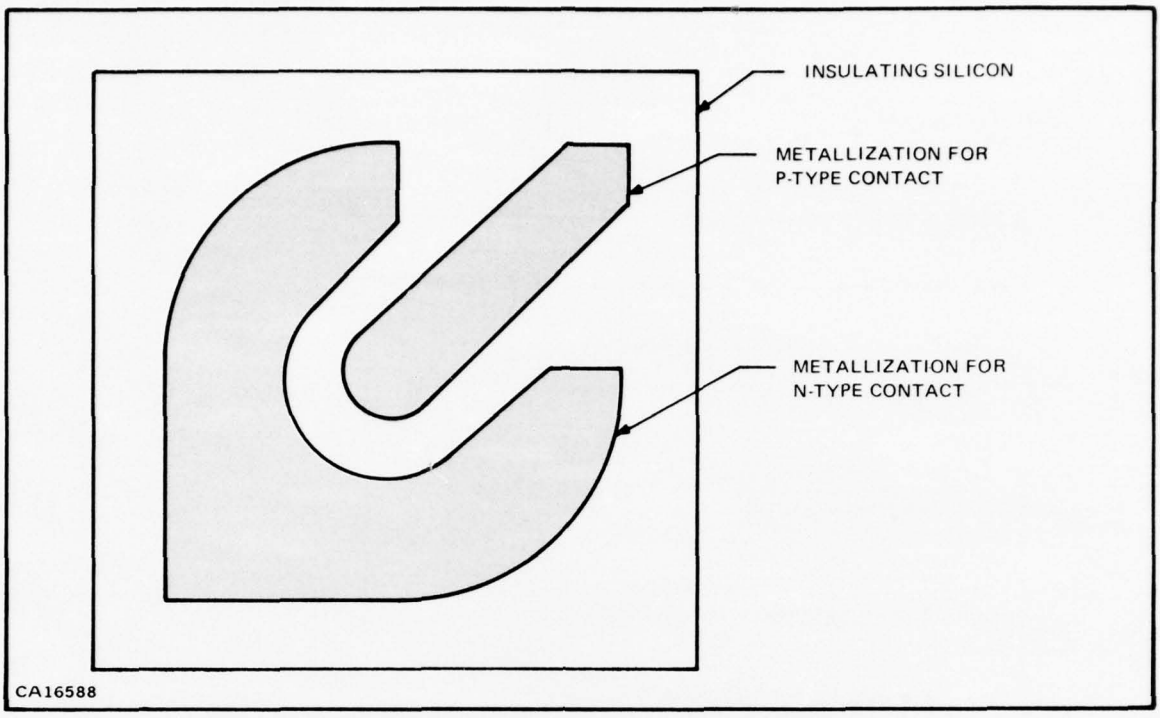

Figure 8. Schematic View of Silicon Submount–Insulating Silicon with Au Metallization on Top

These headers will directly fit the infrared illuminator system delivered on Contract No. DAAK02-67-C-0583. For a description of this system see Final Report No. 03-68-56. The data for the two arrays is given in Table V.

During the time period following the conclusion of Contract No. DAAK02-67-C-0583 to the end of the present contract, a total of 58 GaAsP slices have been grown and processed for dome emitters. Five additional slices were grown but not processed due to an accidentally low doping concentration resulting in high resistivity. The results of the work done of 47 of the 58 slices are given in the following sections. The other 11 slices are still in processing at the present time.

One of the aims of the contract work was the optimization of the junction formation technique. To this end, effort was applied toward forming the PN junction using silicon nitride (Si_3N_4) as the diffusion mask. Heretofore, the diffusion mask used has been silicon dioxide (SiO_2) doped with phosphorous. However, SiO_2 did not constitute a satisfactory mask since considerable lateral diffusion occurred around the edges of the hole in the SiO_2. This lateral diffusion precluded exact definition of the PN junction and caused the junction size to be somewhat erratic.

Through the use of Si_3N_4 as the diffusion mask, lateral diffusion is essentially eliminated. This greatly improves the definition of the diffusion areas and thereby increases yield. Exact results of the improvement realized are not yet known since a great amount of difficulty was encountered in reducing this technique to actual practice and the first slices successfully processed in this manner are not yet completed.

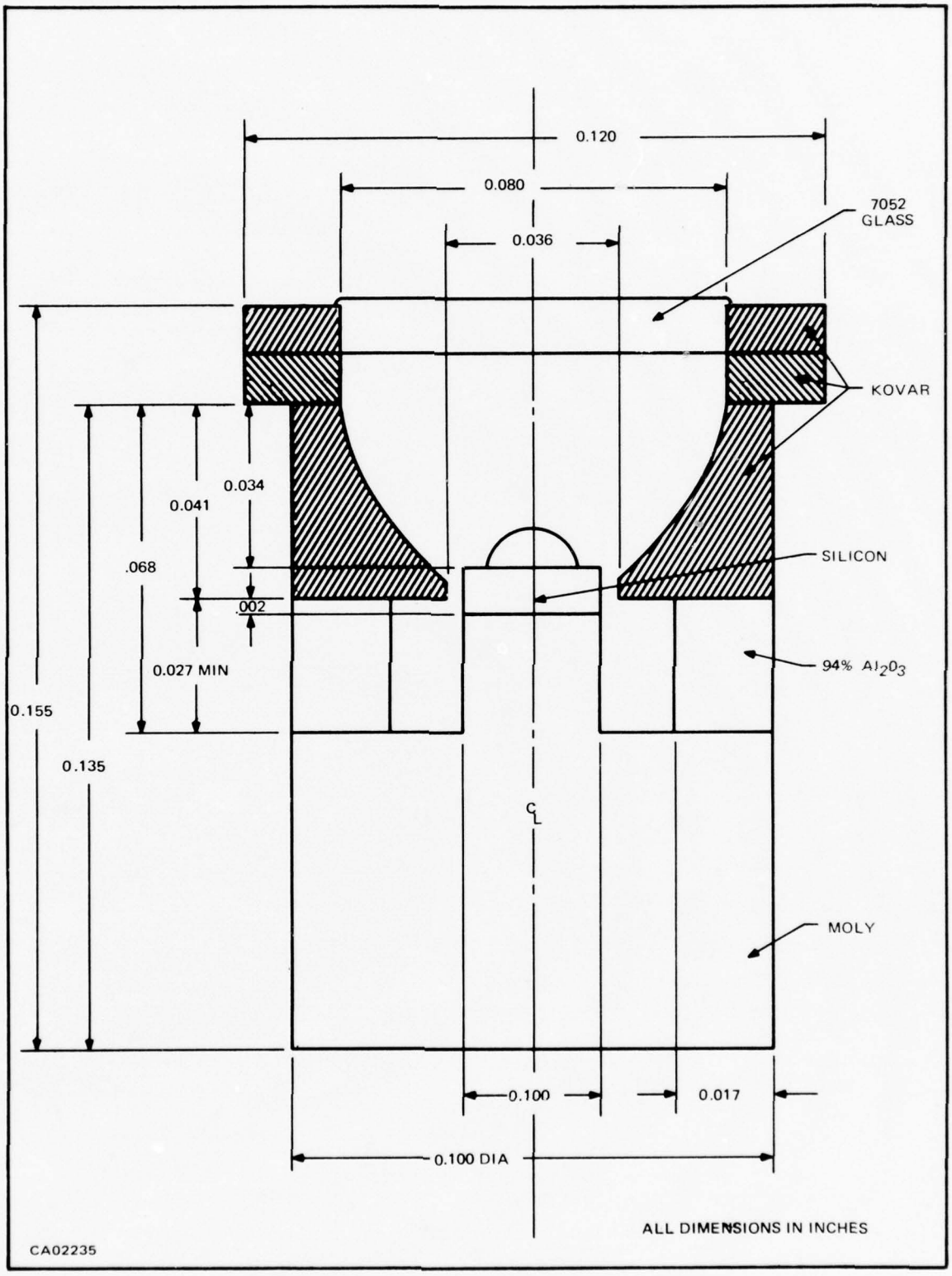

Figure 9. Emitter Package Design–Alternate 2

Table III. Data Taken on First Group of Devices Delivered

All data taken at I_f = 200 mA						
Device No.	V_f (V)	Light Out (mA)	η_Q (%)	λ (Å)	Power Out (mW)	η_P (%)
1465–3	2.06	6.88	3.4	8530	10.0	2.4
1465–4	1.62	6.95	3.5	8520	10.1	3.1
1465–6	1.86	8.12	4.1	8470	11.9	3.2
1465–9	1.66	7.50	3.8	8600	10.8	3.3
1465–14	1.70	7.59	3.8	8570	11.0	3.2
1465–15	1.72	7.37	3.9	8580	10.6	3.3
1465–16	1.65	7.14	3.6	8550	10.4	3.2
1465–22	1.62	7.28	3.6	8570	10.5	3.2
1465–27	1.54	9.15	4.6	8580	13.2	4.3
1465–30	1.69	7.27	3.6	8620	10.5	3.1

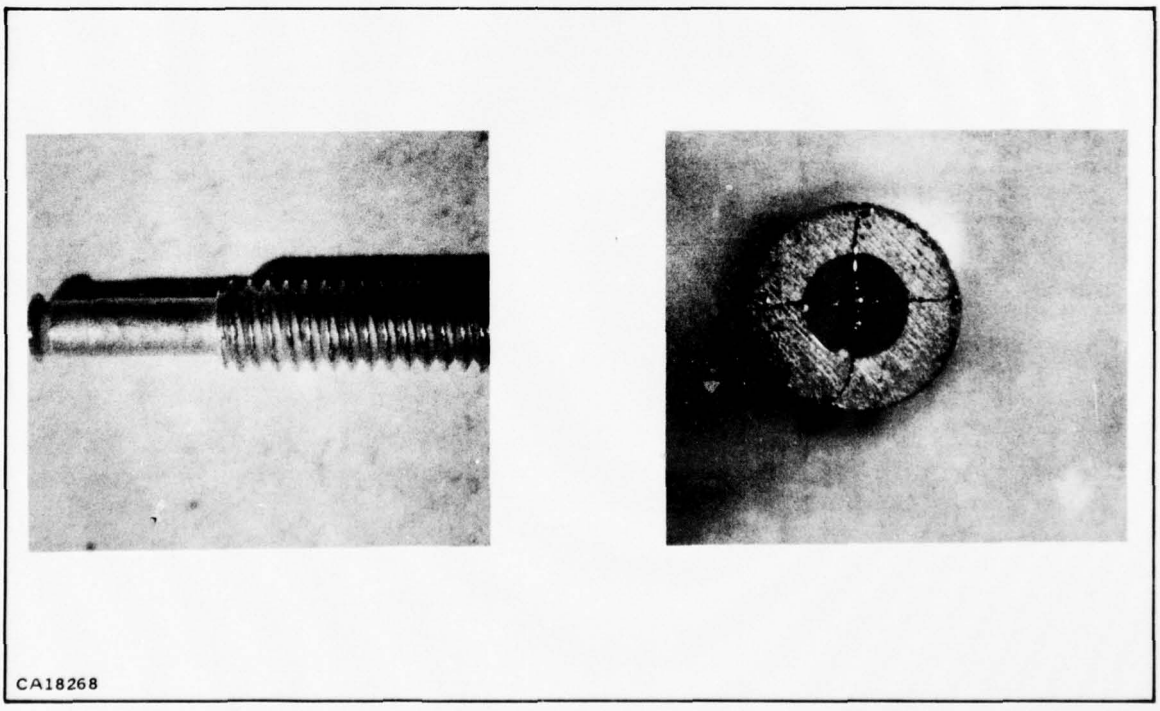

Figure 10. Header Developed for GaAsP Hemispherical Light Emitting Diodes

Table IV. Data Taken on Second Group of Devices Delivered

All data taken at I_f = 200 mA						
Device No.	V_f (V)	Light Out (mA)	η_Q (%)	λ (Å)	Power Out (mW)	η_P (%)
1462–1	1.54	9.18	4.6	8555	13.3	4.3
1462–2	1.55	8.52	4.3	8495	12.4	4.0
1462–5	1.55	7.40	3.7	8500	10.7	3.5
1462–6	1.54	8.96	4.5	8540	13.0	4.2
1462–8	1.54	11.2	5.6	8545	16.2	5.3
1462–12	1.57	7.02	3.5	8540	10.2	3.3
6937–4	1.56	8.96	4.5	8380	13.2	4.2
6937–5	1.57	7.98	4.0	8350	11.7	3.7
6940–2	1.93	7.20	3.6	8330	10.5	2.7
6940–7	1.83	6.79	3.4	8330	10.1	2.8

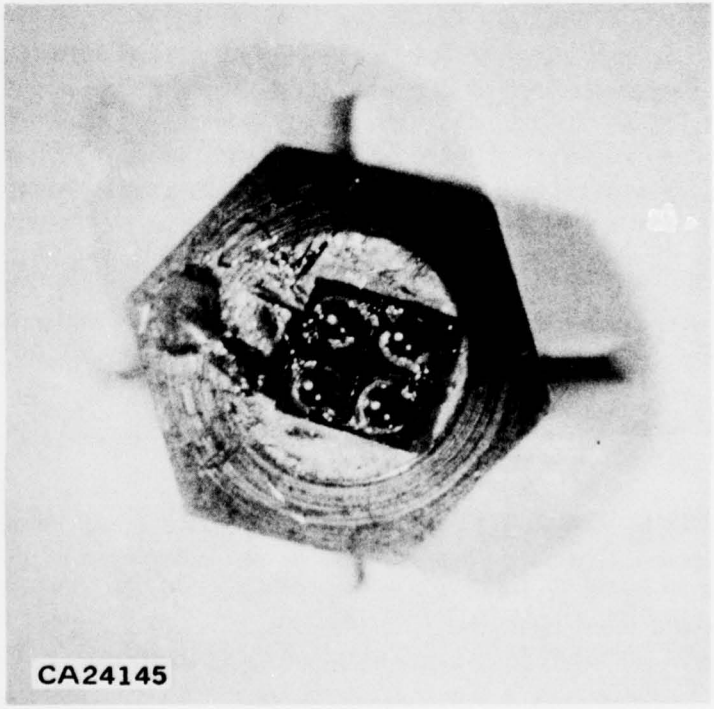

Figure 11. Four-Element Array Source

Table V. Data Taken on Four-Element Arrays

I_f (mA)	V_f (V)	L.O. (mA)	O.P. (mW)	η_Q (%)	η_P (%)	λ_P (Å)	$-\lambda_{1/2}$ (Å)	$+\lambda_{1/2}$ (Å)
Array No.1								
50	6.83	6.94	10.4	13.9	3.05	8240	8185	8315
100	7.48	16.80	25.2	16.8	3.37	8280	8205	8350
150	7.90	26.80	40.0	17.9	3.38	8290	8230	8380
200	8.25	36.10	53.8	18.0	3.26	8315	8260	8415
Array No.2								
50	6.85	6.16	9.25	12.3	2.70	8250	8195	8312
100	7.50	15.00	22.5	15.0	3.00	8270	8215	8340
150	8.00	23.90	35.8	15.9	2.98	8285	8230	8370
200	8.40	32.8	49.0	16.4	2.92	8305	8255	8395

The Si_3N_4 layer is deposited following slice polish and cleanup. The slice is polished using a Clorox etch–mechanical buff technique. Following polish, and immediately prior to Si_3N_4 deposition, the slice is cleaned in a sulfuric acid–hydrogen peroxide mixture followed by a quick dip in hydrofluoric acid.

The problem arises in the removal of the Si_3N_4 from the areas where the diffusion is to be made and where the contacts are later to be applied. The Si_3N_4 layer is much more difficult to etch than the previous SiO_2. Thus, the initial attempts to use Si_3N_4 in a manner similar to that used on SiO_2 failed because the surface of the GaAsP material in the etched holes was not sufficiently "clean." This made it impossible to form the metal contacts in these areas and make them adhere to the semiconductor surface. The problem was finally solved by first depositing SiO_2 in just those areas of the mask which will later be removed. Then, following the Si_3N_4 deposition, the desired areas are etched out. The last layer to be removed is the SiO_2 which, being relatively easy to etch, is completely removed and leaves the GaAsP surface suitable for applying metallization. The use of the Si_3N_4 as a means of passivation will be discussed in a later section.

B. DEVICE EVALUATION AND CHARACTERIZATION

The devices resulting from the light emitter development work were evaluated and characterized on the basis of electrical and optical performance. A sample batch of units was built from the wafers produced in each processing run made on each slice of material. This sample batch was evaluated with regard to forward voltage versus current characteristics, light output versus forward current, and wavelength versus forward current. In the cases where the pilot evaluation indicated a favorable result, the remaining wafers were used in constructing light emitters.

1. Typical Device Characteristics

Table VI gives the peak output wavelength and quantum efficiency of the best unit out of the evaluation lots for the 48 slices processed since the end of the last contract. These units were all mounted on TO-5 stud headers for evaluation purposes. The peak wavelength is given for a forward current of 200 mA.

One of the best slices seen to date has been No. 6927. Referring to Table VI, it is seen that the best unit had a quantum efficiency of 6.6%. This device had a measured optical power output of 20.3 mW at 200 mA forward bias, which is the highest output to date. The high power output of this unit is even more noteworthy in view of the fact that the peak wavelength is low (8100 Å). Complete characteristics for this unit are given in Table VII.

The fact that the units from Process No. 6927 are very good quality can be further seen in referring to Table VIII. This gives a breakdown of some of the later process runs as to maximum output power and percentiles falling in a particular power output range. As can be seen in this compilation, several of these process runs had a good percentage of units producing 7 mW and over, whereas quite a few produced no units having 7 mW power output. At the present time, the qualitative differences from run to run which give rise to this fact are not known. Therefore, in attempting to produce a number of units which meet certain wavelength and output specifications, the problem becomes one of statistics in which enough process runs are made to enable the desired units to be selected from the total number of devices produced.

2. Device Degradation Studies

At the present time, the problem of device reliability is the major disadvantage of the GaAsP dome emitters. Although a lifetime specification was not a part of this contract, a portion of the contract effort was devoted to the area of reliability. A number of reliability experiments were performed in an effort to identify the cause or causes of the degradation.

One such experiment was performed in order to determine if the type submount used, conducting or insulating, influenced the degradation mechanism. Figures 12 and 13 give the relative light output as a function of time for the best unit and worst unit of groups of devices mounted on both conducting and insulating submounts. In each case, the forward current is 100 mA. As shown by these two pairs of curves, there is little or no difference enountered due to these two types of submounts. This conclusion is also supported in an examination of the thermal impedance of units mounted on both types of submounts.

Table IX gives a comparison of thermal impedances measured on devices mounted on both types of submounts. There are no significant differences to be found since the thermal impedance varies over approximately the same range in both cases. Therefore the amount of degradation does not seem to be a function of the two types of submounts presently in use. For a description of the method of measuring the thermal impedance, see First Interim Report No. 03-68-20, Contract No. DAAK02-67-C-0583.

Table VI. Wavelength and Efficiency for Various Process Runs

Process No.	$Peak_{\eta}$ at 200 mA	η_Q(%) of Best Unit
1459	8550	4.1
1460	8550	1.0
1461	8650	4.9
1462	8525	4.9
1463	8600	1.7
1464	8450	2.5
1465	8450	4.0
1466	8490	2.8
1467	8480	3.3
1468	8550	4.2
1485	8650	1.3
1486	8250	2.4
1487	8175	2.4
1488	8200	3.0
1489	7830	2.2
1490	7920	3.1
1518	8150	1.4
1524	All Shorted Units	
1525	8050	3.5
1526	8040	2.9
1527	8100	<1.0
1530	8040	2.4
1531	Slice ruined in processing	
1532	7980	2.3
1533	8100	<1.0
1537	8050	<1.0
1538	8150	1.4
1539	8300	<1.0
1562	8200	<1.0
1567	No light output	
1568	No light output	
1569	8100	3.3
1570	7950	2.9
1571	8100	1.3
6922	8100	<1.0
6923	8450	2.8
6924	8500	3.5
6925	8450	2.0
6926	8200	1.1
6927	8100	6.6
6934	8200	1.5
6936	8300	3.0
6937	8350	5.4
6939	8300	5.7
6940	8350	3.8
6941	8350	3.8
6942	8200	4.0

Table VII. Characteristics of Unit No. 6927-7

I_f (mA)	V_f (V)	Light Out (mA)	Optical Power (mW)	λ_{peak} (Å)	η_Q (%)	η_P (%)
50	1.46	3.05	4.73	8010	6.11	6.48
100	1.52	6.71	10.4	8026	6.71	6.82
150	1.57	9.82	15.1	8052	6.55	6.42
200	1.62	13.2	20.3	8062	6.59	6.25

Table VIII. Ranges of Power Output for Various Process Runs

Process No.	Peak λ at 200 mA	Peak Power (mW) at 200 mA	% Over 7 mW	% Over 10 mW
1525	8050	10.7	28	14
1526	8040	8.8	30	0
1527	8100	4.5	0	0
1530	8040	7.3	16	0
1532	7980	7.0	16	0
1533	8100	2.5	0	0
1537	8050	3.0	0	0
1538	8150	4.0	0	0
1539	8300	1.5	0	0
1562	8200	1.5	0	0
1569	8100	10.4	50	12
1570	7950	9.5	10	0
1571	8100	4.0	0	0
6922	8100	2.5	0	0
6923	8450	8.1	20	0
6924	8500	10.2	73	6
6925	8450	5.7	0	0
6926	8200	3.5	0	0
6927	8100	20.2	90	33
6934	8200	5.1	0	0
6936	8300	8.9	20	0
6937	8350	15.7	100	75
6939	8300	17.0	58	42
6940	8350	11.2	82	45
6941	8350	11.3	55	33
6942	8200	12.1	30	14

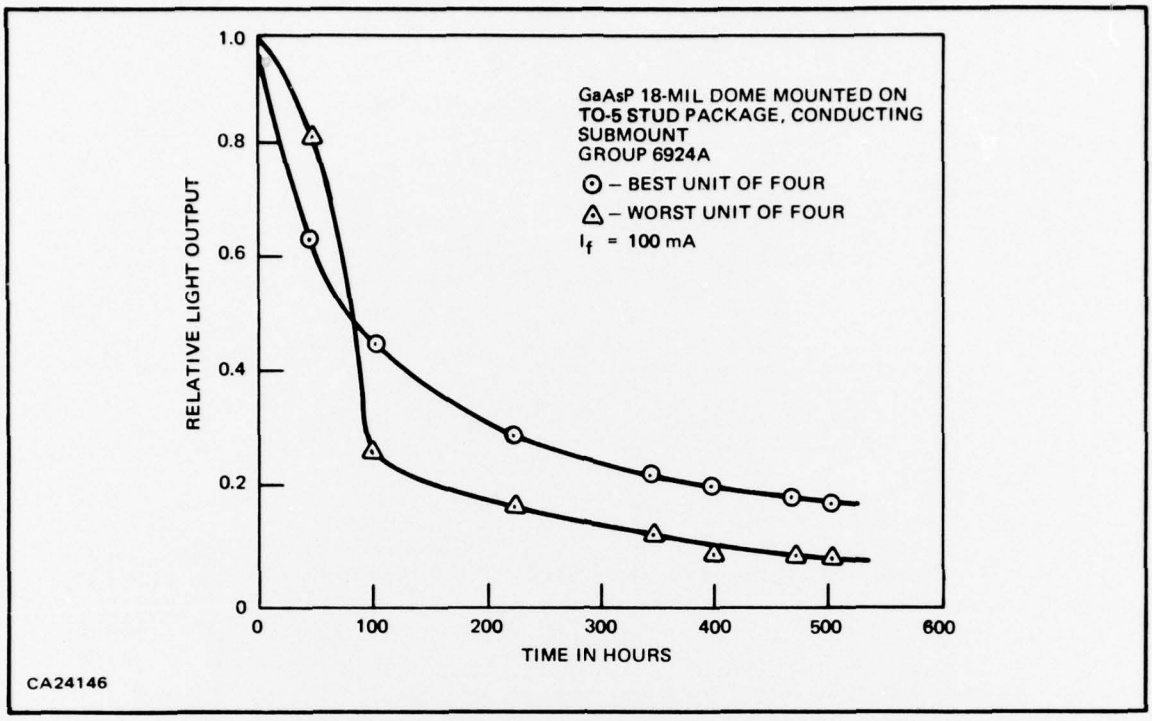

Figure 12. Relative Light Output versus Time–Conducting Submounts

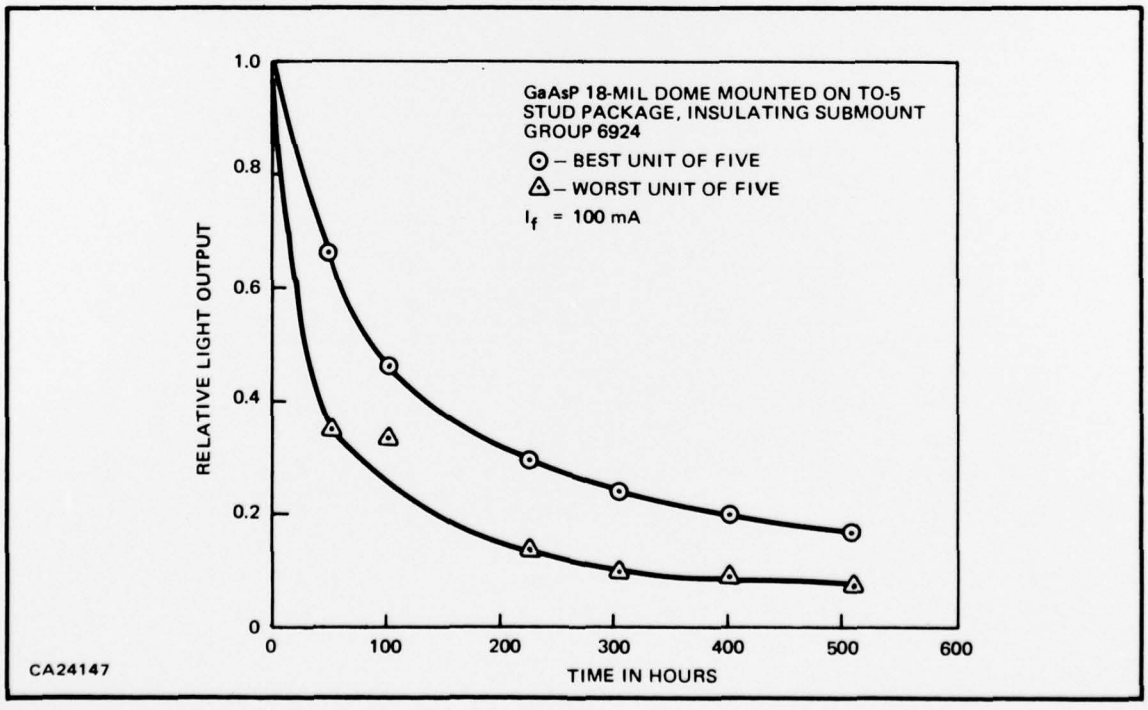

Figure 13. Relative Light Output versus Time–Insulating Submounts

Table IX. Thermal Impedance for Conducting and Insulating Submounts

Unit No. (Conducting Submounts)	Thermal Impedance (°C/W)	Unit No. (Insulating (Submounts)	Thermal Impedance (°C/W)
830–2	64	6940–1	96
830–4	212	6940–2	110
994–1	84	6940–3	170
994–2	180	6940–4	43
1034–2	137	6940–5	49
1034–6	172	6940–6	67
1118–2	63	6940–7	180
1118–3	63		
1118–4	63		
1118–5	46		
1119–1	56		
1119–2	70		
1119–3	100		
1119–4	114		
1119–5	159		
1119–6	87		
1134–1	60		
1134–5	71		
1135–1	71		
1135–2	93		
1135–4	74		
1135–5	74		
1135–6	64		

Figures 14 and 15 give the relative light output versus time for two groups of units mounted on conducting submounts and operated at 200 mA forward current. However, in this case, the group of Figure 15 were sealed by applying varnish around the circumference of the dome at the place where it interfaces the submount. The varnish used is of the type used in sealing the junctions of GaAs mesa-type units. It appears from the curves that this procedure may have reduced the degradation to some extent. However, since a fairly low number of units were involved, it is difficult to make a qualified judgment. More work in this area is required in order to determine if this procedure can be applied in solving the degradation problem.

Another procedure aimed at reducing the degradation was to alter the method of bonding the dome to the submount. In the device laboratory, this is a soldering step done by hand on a strip heater and with the use of solder flux. It has been felt that the flux could be one of the sources of the problem. Therefore, in an attempt to determine this, a group of domes and submounts were bonded by means of an automated furnace process used in the assembly of the TIL09 line of commercial GaAs 18-mil diameter dome emitters. In this process there is no solder flux involved. A group of devices from the same slice of material was fabricated in the usual manner in order to

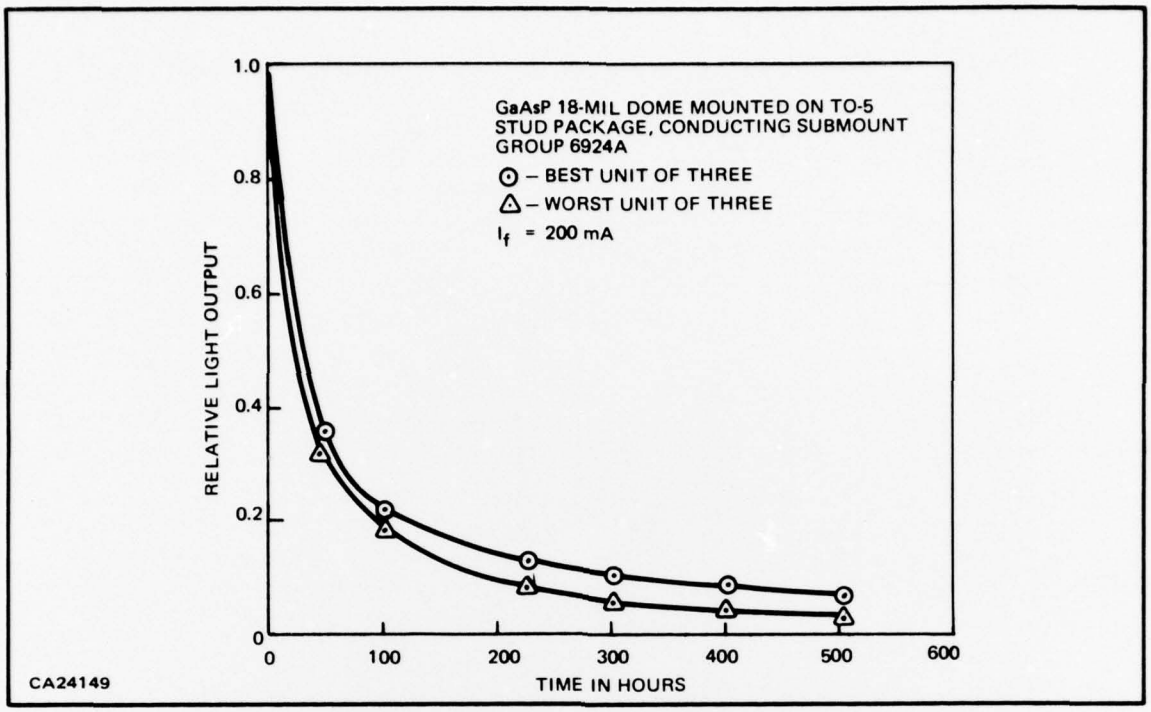

Figure 14. Relative Light Output versus Time–Conducting Submounts

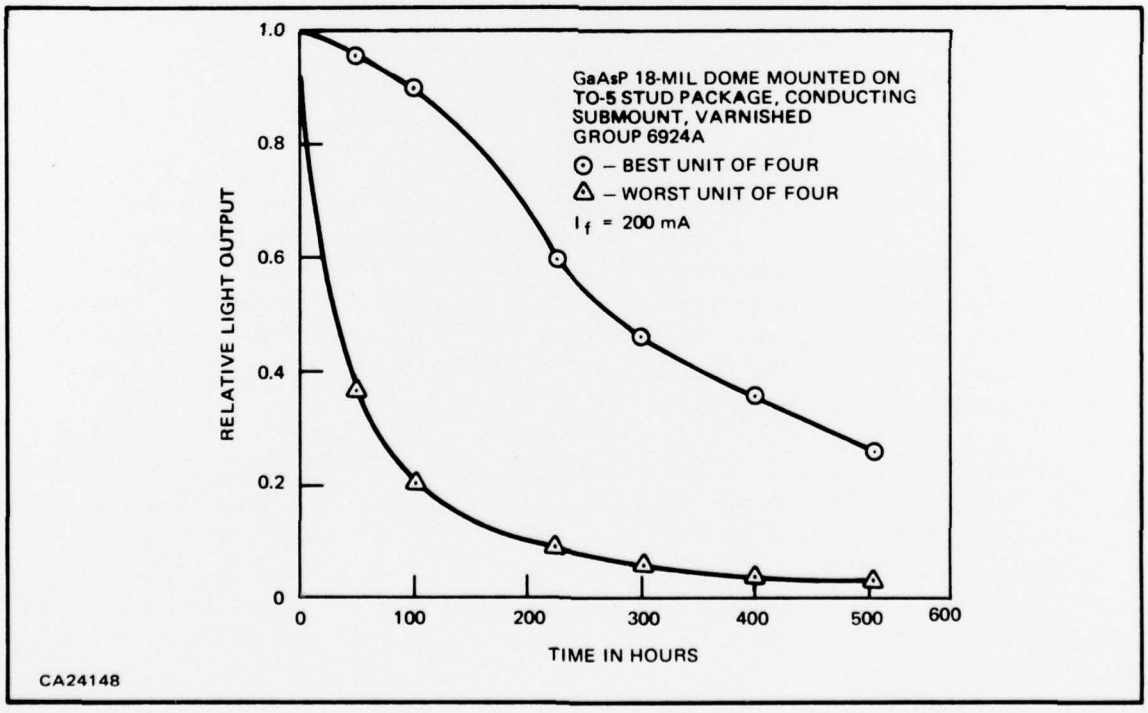

Figure 15. Relative Light Output versus Time–Varnished Conducting Submounts

provide a control. The results of a 100 hour life test are shown in Figures 16 and 17. Figure 16 gives the results of the units mounted in the usual manner, and Figure 17 shows the degradation of the units fabricated using no solder flux. All devices were biased at 200 mA forward current. In comparing the two groups of curves, there appears to be no significant difference in the device degradation which can be attributed to the presence or absence of solder flux in the dome-to-submount assembly process. A point to be noted in this regard is that the furnace assembly process presently being used in the TIL09 device manufacture has been shown to produce units which statistically exhibit less degradation than units assembled by hand using solder flux. In light of this, it seems quite likely that further experimentation in this area would show the same behavior in the GaAsP devices.

As previously mentioned, it also seems quite likely that an improvement in device lifetime may be realized through the use of Si_3N_4 surface passivation. Surface passivation using Si_3N_4 was found to be very effective in the case of silicon devices, and there is no reason to believe that it would not be equally effective for GaAs and GaAsP. However, this has not yet been shown. Because of the problems involved in the Si_3N_4 processing, explained previously, attempts at fabricating devices have been unsuccessful. At the present time, a group of slices have had contacts applied successfully using the method described, and it seems likely that they will yield finished devices having Si_3N_4 as a passivation agent. These devices will be placed on life test in order to determine if the expected improvement in device lifetime is, indeed, realized.

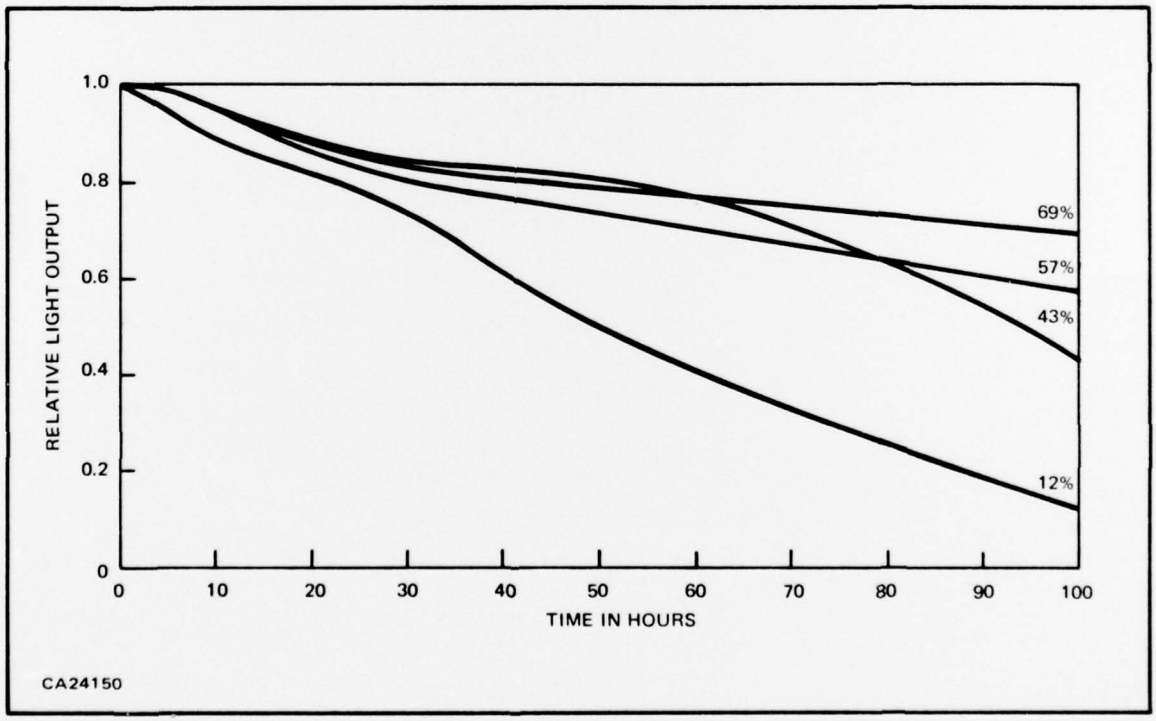

Figure 16. Degradation with Time for Domes Assembled on Submounts Using Solder Flux

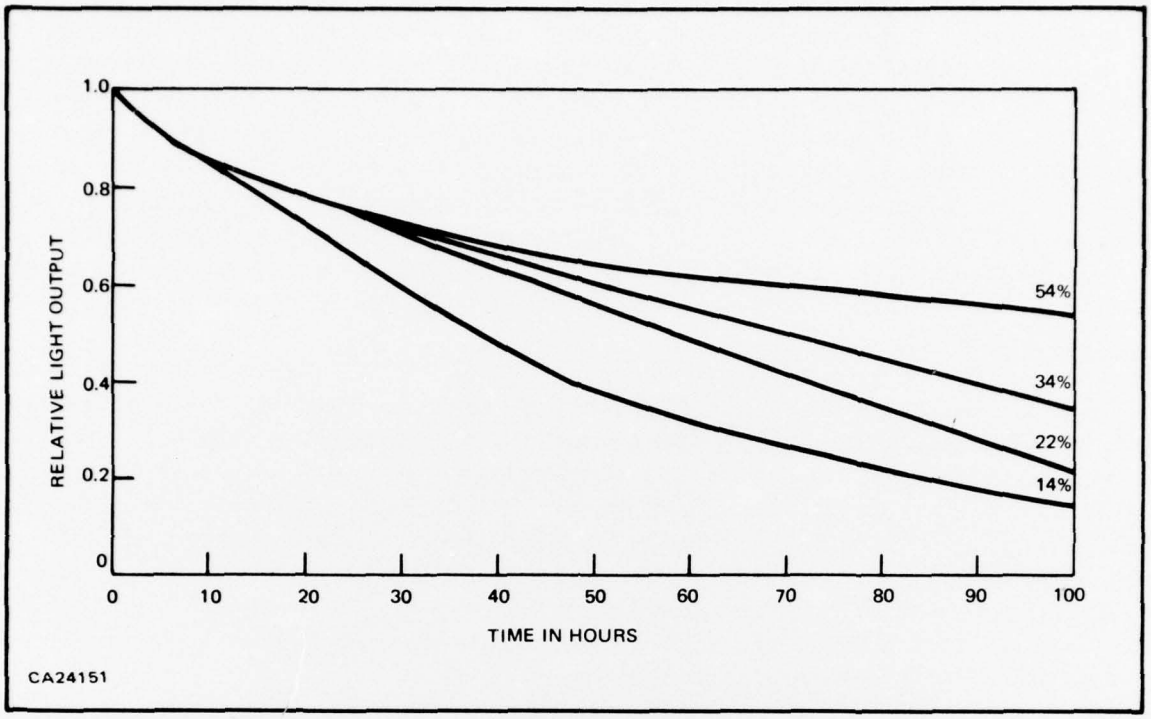

Figure 17. Degradation with Time for Domes Assembled on Submounts Using No Solder Flux

SECTION III

CONCLUSIONS AND RECOMMENDATIONS

Device quality slices of $GaAs_{1-x}P_x$ material have been prepared by chemical vapor epitaxial deposition with values of x ranging from 0.01 to 0.18. Both selenium and sulfur have been successfully used as a dopant. Hemispherical shaped junction light emitters were fabricated from this material with a quantum efficiency as high as 6.6%. Emission wavelengths from 7800Å to 8600Å were demonstrated.

The principal area for further work on GaAsP dome emitters is on the problem of device degradation. Although some work in this area has been done, a thorough investigation into the causes of the degradation and the solutions to the problem is necessary. Work performed at Texas Instruments in the area of visible light emitters formed in GaAsP indicates that fairly stable devices can be fabricated from this material. Life tests have been conducted on such devices out to several thousand hours in which the degradation in light output has reached only a few percent. Since these devices are fabricated by a completely different process from dome emitters, the indication is that one particular area of investigation should be that of device processing techniques.

A great deal of work needs to be done in a study of the diffusion technology in GaAsP. A technique for forming the junctions in dome emitters by a method similar to that used on P-side-up emitters can be developed which may help solve the degradation problem.

Further work in the area of surface passivation needs to be carried out. The Si_3N_4 layers were originally used to eliminate the lateral diffusion and properly define the desired junction areas during diffusion. The passivation characteristics of Si_3N_4 on GaAsP have not been thoroughly investigated.

Other areas of processing technology in device fabrication such as cleanup procedures, ohmic contact application, and device assembly techniques require further refinement. Besides the investigation of processing procedures, a continuing effort towards further improvements in the materials preparation area is most important.

SECTION IV

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13 ABSTRACT

Investigations were performed in an effort to extend the state-of-the-art of GaAsP light emitters and emitter arrays. This effort included a materials study aimed at providing usable GaAsP capable of yielding high quantum and power efficiency at the desired wavelength. The effort also consisted of a study of processing and fabrication techniques to take full advantage of the material capabilities. Device quality slices of $GaAs_{1-x}P_x$ material have been prepared by chemical vapor epitaxial deposition with values of x ranging from 0.01 to 0.18. Both selenium and sulfur have been successfully used as a dopant. Hemispherical shaped junction light emitters were fabricated from this material with a quantum efficiency as high as 6.6%. Emission wavelengths from 7800Å to 8600Å were demonstrated. At the present time, the problem of device degradation has been found to be the main area in which further effort is required.

GaAs(1-x)P(x)

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Security Classification

14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Quantum efficiency						
Optical power output						
Silicon submount						
Doping level						
Graded junction						
Device reliability						

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